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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,564	11/24/2003	Phillip J. Restle	YOR920030455US1	5729

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,564	RESTLE, PHILLIP J.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *8-11 and 21-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,12-16 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/720,809, Response to Election/Restriction filed on 07/28/2006, and Amendment filed on 05/23/2006. Applicants have elected claims 1-7, and 12-20 (Group 1) without traverse. Claims 8-11 and 21-27 (Group 2) are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected. Dependent claims 6 and 16 have been amended. Claims 1-7 and 12-20 remain pending in the application.

The Examiner finds Applicant's arguments on the applications of Shepard as none persuasive. Shepard's reference reads on the claims 1-7 and 12-20 as presently written.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7, 12-16 and 18-20 are rejected under 35 U.S.C. 102(e) as being unpatentable by Shepard et al. (US Pub. No.: 20050057286).

3. As to claims 1 and 12 Shepard discloses:

(1) An integrated circuit (IC) comprising:

a clock distribution grid distributing a clock to local circuits, said distribution grid (The circuit of FIG. 1A illustrates the four sectors 101 being driven by a further clock distribution circuit, such as an H-tree 102, to deliver the clock signal from a master clock 103 to the individual sector driver circuits) having a known load capacitance (the capacitance of the clock distribution circuit can be tuned by including one or more capacitors which can be selectively switched into or out of the clock distribution circuit to optimize the circuit resonance) ([0023]-[0024]; [0033] ;[0037]);

a clock driver driving said clock distribution grid (a clock signal driver coupled to the resonant circuit for driving a clock signal on the clock distribution grid) ([0033]; claim 21);

at least one inductor connected at one end to said distribution grid (the spiral inductors 120 have one end coupled directly to the clock grid 125), said clock having a frequency within the frequency range of the resonant frequency of local grid capacitance and said at least one connected inductor (The spiral inductors 120 are formed with a spiral length, spacing and line width to present an inductance value that will substantially resonate with the capacitance presented by the clock tree 115 and clock grid 125 at the desired clock frequency) ([0019]; [0034]; [0036]; claim 9); and

a power grid, power grid lines being discontinuous in the vicinity of each said at least one inductor, whereby power grid line loops are open in the vicinity of each said at least one inductor (Because the spiral inductors are generally much larger than the power grid, most of the potential deleterious coupling will be to the underlying power grid. To reduce eddy current formation in the underlying grid, the vias in the grid can be

dropped and small cuts can be made in the wires. This technique is generally known to those skilled in the art of RF circuit design as it is analogous to ground plane laminations used for spiral inductors in RF circuits) ([0035; [0039).

(12) An integrated circuit (IC) assembly clocked by a global clock, said global clock being distributed to a plurality of sectors (A typical microprocessor clock distribution may include several dozen of such clock distribution sectors, which are coupled together to provide a global clock distribution circuit- [0033]), each of said sectors comprising:

a clock distribution grid distributing a clock to local circuits, said distribution grid (The circuit of FIG. 1A illustrates the four sectors 101 being driven by a further clock distribution circuit, such as an H-tree 102, to deliver the clock signal from a master clock 103 to the individual sector driver circuits) having a known load capacitance (the capacitance of the clock distribution circuit can be tuned by including one or more capacitors which can be selectively switched into or out of the clock distribution circuit to optimize the circuit resonance) ([0023]-[0024]; [0033] ;[0037]);

a clock driver driving said clock distribution grid (a clock signal driver coupled to the resonant circuit for driving a clock signal on the clock distribution grid) ([0033]; claim 21);

at least one inductor connected at one end to said distribution grid (the spiral inductors 120 have one end coupled directly to the clock grid 125), said clock having a frequency within the frequency range of the resonant frequency of local grid

capacitance and said at least one connected inductor (The spiral inductors 120 are formed with a spiral length, spacing and line width to present an inductance value that will substantially resonate with the capacitance presented by the clock tree 115 and clock grid 125 at the desired clock frequency) ([0019]; [0034]; [0036]; claim 9); and

a power grid, power grid lines being discontinuous in the vicinity of each said at least one inductor, whereby power grid line loops are open in the vicinity of each said at least one inductor (Because the spiral inductors are generally much larger than the power grid, most of the potential deleterious coupling will be to the underlying power grid. To reduce eddy current formation in the underlying grid, the vias in the grid can be dropped and small cuts can be made in the wires. This technique is generally known to those skilled in the art of RF circuit design as it is analogous to ground plane laminations used for spiral inductors in RF circuits) ([0035; [0039);

4. As to claims 2-7, 13-16 and 18-20 Shepard recites:

(2), (13) An IC/assembly, wherein said at least one inductor is connected to a decoupling capacitor (decap) at an other end ([0040]);

(3), (14) An IC/assembly, wherein a voltage develops across each said decap, said voltage being midway between a high level and low level of said clock (mid-rail voltage) ([0034]);

(4), (5), (15), (16) An IC/assembly, wherein a first of said pair being connected between a first supply line and said other end of said inductor and an other of said pair being connected between said other end and a second supply line ([0028]; [0034]; [0037]; [0039]; [0042]; claim 7; Figs. 1-4);

(6) An IC, wherein said power grid lines include supply and supply return lines terminating on endpoints ([0028]; [0037]; [0039]; [0042]; Figs. 1-4);

(7), (20) An IC/assembly, wherein at least one inductor is four inductors located in four quadrants around said clock driver ([0033]; [0034]; [0043]);

(18) An IC/assembly further comprising a pair of cross coupled inverters ([0012]);

(19) An IC/assembly further comprising a second clock driver driving said second clock phase ([0034]; [0047]; [0055]).

Allowable Subject Matter

5. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

An integrated circuit (IC) assembly clocked by a global clock, said global clock being distributed to a plurality of, each of said sectors comprising:

a clock distribution grid distributing a clock to local circuits, said distribution grid having a known load capacitance;

a clock driver driving said clock distribution grid ;

at least one inductor connected at one end to said distribution grid, said clock having a frequency within the frequency range of the resonant frequency of local grid capacitance and said at least one connected inductor;

a power grid, power grid lines being discontinuous in the vicinity of each said at least one inductor, whereby power grid line loops are open in the vicinity of each said at least one inductor; and

wherein said clock driver is driving a first clock phase, said one end of said at least one inductor being connected to said first clock phase, said IC further comprising:

a second clock phase, said at least one inductor being connected to said second phase at an other end, said load grid capacitance comprising local wiring capacitance from both of said first clock phase and said second clock phase.

REMARKS

5. Mostly Applicant argues: "A general statement of making "small cuts can be made in the wires" does not imply a power grid with discontinuous grid lines "in the vicinity of each said at least one inductor" as claims 1 and 12 recite, much less as amended claims 6 and 16 specifically recite. Therefore. Shepard el al. fails to teach or suggest the present invention as recited in claims 1 and 12 or, further, in claims 6 and 16."

6. As to claims 1 and 12 Shepard, for example, teaches: "Because the spiral inductors are generally much larger than the power grid, most of the potential deleterious coupling will be to the underlying power grid. To reduce eddy current formation in the underlying (power) grid, the vias in the (power) grid can be dropped and small cuts can be made in the wires - paragraph 39". In this passage the term "the vias in the (power) grid can be dropped and small cuts can be made in the wires" corresponds to the Applicants term "a power grid with discontinuous grid lines" because

vias are dropped in the power grid and to allow vias go through power grid, it is necessary to discontinue wires, which are the grid lines.

Shepard explains in the same paragraph that discontinue of grid lines "in the vicinity of each said at least one inductor" means, e.g.: "This technique is generally known to those skilled in the art of RF circuit design as it is analogous to ground plane **laminations** used for spiral inductors in RF circuits - paragraph 39". The term "**laminate**" should be explained in this passage as "1) *intransitive verb:* to separate into laminae and 2) *intransitive verb*: to divide into laminae" (please see http://www.m-w.com/cgi-bin/dictionary). Thereby "ground plane **laminations** used for spiral inductors" in Shepard corresponds to "a power grid with discontinuous grid lines in the vicinity of each said at least one inductor" in Applicants claims.

7. As to claims 6 and 16 Shepard's reference reads on the claims 6 and 16 as presently written. The arguments presented above, Fig. 2 and paragraphs 28, 37 also, e.g., shows "a perspective view illustrating the fingering and shielding of clock grid wires which maintains a low stray inductance in the clock circuit" as recited in amended claims 6 and 16 and Fig.2 of the Applicants' Specification.

8. Examiner defined Applicant's arguments as none persuasive.

Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VUTHE SIEK
PRIMARY EXAMINER